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DATA SHEET

TZA3000
SDH/SONET STM4/OC12 optical receiver

Objective specification
File under Integrated Circuits, IC19

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Philips Semiconductors

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SDH/SONET STM4/OC12 optical receiver TZA3000

FEATURES

- Low equivalent input noise, typically 3.5 pA/√Hz
- Wide dynamic range, typically 1 μA to 1.5 mA
- On-chip low-pass filter. The bandwidth can be varied between 370 and 600 MHz using an external resistor. Default value is 470 MHz.
- Differential transimpedance of 1.8 MΩ
- On-chip AGC (Automatic Gain Control)
- PECL (Positive Emitter-Coupled Logic) or CML (Current-Mode Logic) compatible data outputs
- LOS (Loss-Of-Signal) detection
- LOS threshold level can be adjusted using a single external resistor
- On-chip DC offset compensation
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

DESCRIPTION

The TZA3000 optical receiver is a low-noise transimpedance amplifier with AGC plus a limiting amplifier designed to be used in SDH/SONET fibre optic links. The TZA3000 amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3000HL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3000U	naked die	die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM

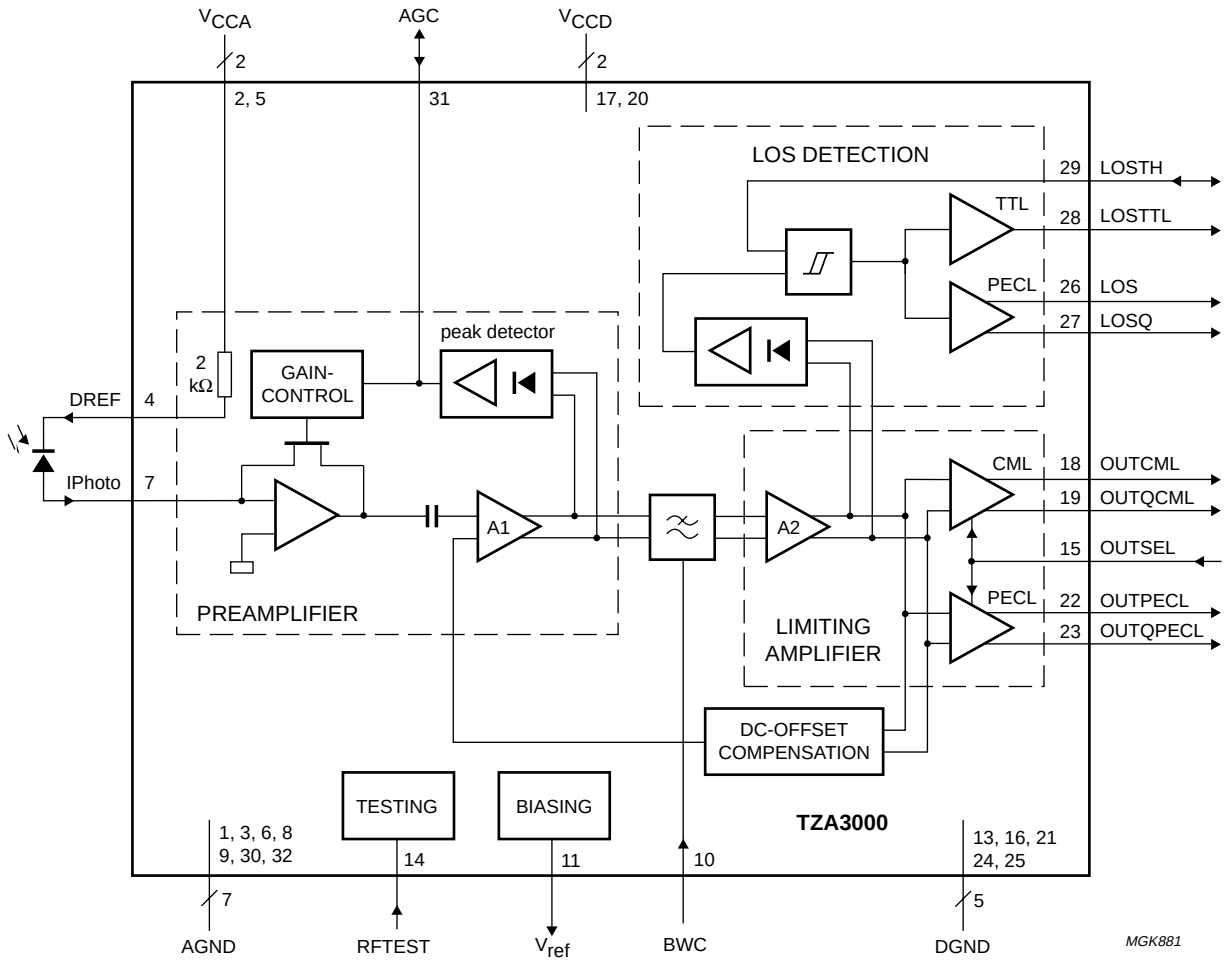


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
AGND	1	ground	analog ground
V_{CCA}	2	supply	analog supply voltage
AGND	3	ground	analog ground
DREF	4	analog output	bias voltage for PIN diode (V_{CCA}); cathode should be connected to this pin
V_{CCA}	5	supply	analog supply voltage
AGND	6	ground	analog ground
IPhoto	7	analog input	current input; connect the anode of PIN diode to this pin; DC bias level is 800 mV, one diode voltage above ground
AGND	8	ground	analog ground
AGND	9	ground	analog ground
BWC	10	analog input	bandwidth control pin; default bandwidth is 470 MHz; a resistor should be connected between V_{ref} (pin 11) and BWC (pin 10) to decrease bandwidth, or between BWC (pin 10) and AGND to increase bandwidth
V_{ref}	11	analog output	band gap reference voltage; nominal value approximately 1.2 V
SUB	12	substrate	substrate pin; to be connected to AGND
DGND	13	ground	digital ground
RFTEST	14	analog input	test pin; not used in application; not connected
OUTSEL	15	CMOS input	output select pin; when OUTSEL is HIGH, CML data outputs are active and PECL data outputs are disabled; OUTSEL is pulled LOW if left unconnected, PECL data outputs will then be active and CML data outputs disabled
DGND	16	ground	digital ground
V_{CCD}	17	supply	digital supply voltage
OUTCML	18	CML output	CML data output; OUTCML goes HIGH when current flows into IPhoto (pin 7)
OUTQCML	19	CML output	CML compliment of OUTCML (pin 18)
V_{CCD}	20	supply	digital supply voltage
DGND	21	ground	digital ground
OUTPECL	22	PECL output	PECL data output; OUTPECL goes HIGH when current flows into IPhoto (pin 7)
OUTQPECL	23	PECL output	PECL compliment of OUTPECL (pin 22)
DGND	24	ground	digital ground
DGND	25	ground	digital ground
LOS	26	PECL output	PECL-compatible LOS detection pin; LOS output is HIGH when the input signal is below the user programmable threshold level
LOSQ	27	PECL output	PECL compliment of LOS
LOSTTL	28	TTL output	CMOS-compatible LOS detection pin; the LOSTTL output is HIGH when the input signal is below the user programmable threshold level
LOSTH	29	analog I/O	pin for setting input threshold level; nominal DC voltage is V_{CCA} – 1.5 V; threshold level set by connecting an external resistor between LOSTH and V_{CCA} or by forcing a current into LOSTH; default value for this resistor is 86 kΩ
AGND	30	ground	analog ground
AGC	31	analog I/O	AGC monitor voltage; the internal AGC circuit can be disabled by applying an external voltage to this pin
AGND	32	ground	analog ground

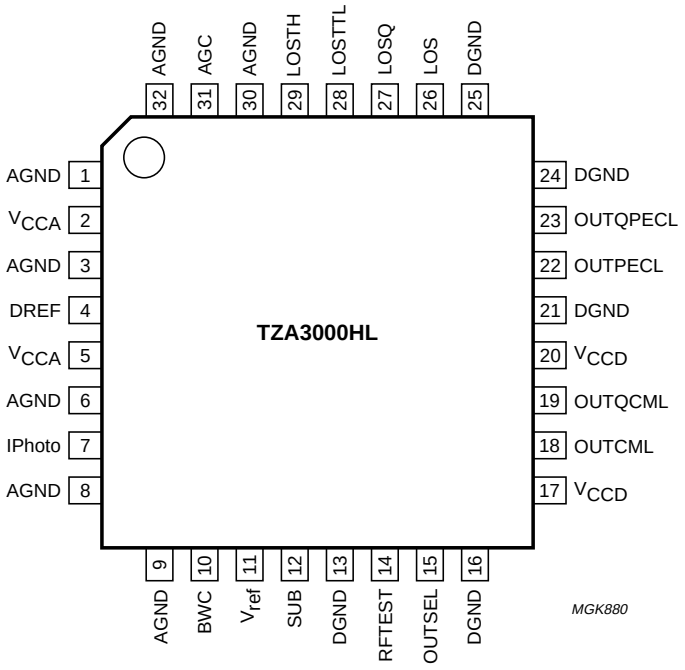


Fig.2 Pin configuration.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES(1)	
		x	y
AGND	1	102	1251
V_{CCA}	2	102	1111
AGND	3	102	971
DREF	4	102	814
V_{CCA}	5	102	674
AGND	6	102	534
IPhoto	7	102	395
AGND	8	102	254
AGND	9	243	105
BWC	10	383	105
V_{ref}	11	523	105
SUB	12	663	105
DGND	13	803	105
RFTEST	14	943	105
OUTSEL	15	1100	105
DGND	16	1257	105
V_{CCD}	17	1398	263
OUTCML	18	1398	403

SYMBOL	PAD	COORDINATES(1)	
		x	y
OUTQCML	19	1398	543
V_{CCD}	20	1398	683
DGND	21	1398	823
OUTPECL	22	1398	963
OUTQPECL	23	1398	1103
DGND	24	1398	1243
DGND	25	1283	1400
LOS	26	1143	1400
LOSQ	27	986	1400
LOSTTL	28	829	1400
LOSTH	29	671	1400
AGND	30	514	1400
AGC	31	357	1400
AGND	32	217	1400

Note

1. All coordinates are referenced, in μm, to the bottom left-hand corner of the die.

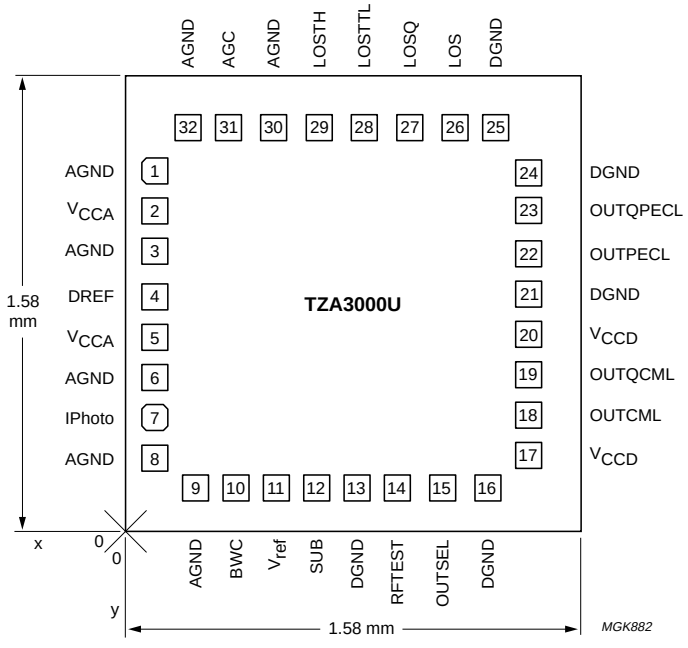


Fig.3 Bonding pad locations: TZA3000U.

FUNCTIONAL DESCRIPTION

The TZA3000 contains five functional blocks:

- Preamplifier input stage
- Low-pass filter
- Limiting amplifier stage
- Offset compensation loop
- Loss-of-signal detection unit.

Preamplifier

The preamplifier provides low-noise amplification of the current generated by a photodiode connected to the IPhoto pin.

A differential amplifier converts the output of the preamplifier to a differential voltage. An AGC loop increases the dynamic range of the receiver by reducing the feedback resistance of the preamplifier. The AGC loop hold capacitor is integrated on-chip, so an external capacitor is not needed for AGC. The AGC voltage can be monitored at pin 31. This pin can be left unconnected for normal operation. It can also be used to force an external AGC voltage. If pin 31 (AGC) is connected to AGND, the internal AGC loop is disabled and the receiver gain is at a maximum. In this case, the maximum input current is about 50 μA.

Low-pass filter

A low-pass filter controls the bandwidth of the receiver, which can be varied between 300 and 600 MHz.
The bandwidth is set to 470 MHz by default. It can be decreased by connecting a resistor between BWC (pin 10) and V_{ref} (pin 11) or increased by connecting a resistor between BWC and AGND.

Limiting amplifier

A limiting amplifier boosts the signal up to PECL levels. The output can be either CML or PECL compatible, selected by means of pin OUTSEL. When OUTSEL is HIGH, CML data outputs are active and PECL data outputs are disabled. If OUTSEL is left unconnected, it is pulled LOW and PECL data outputs are active while CML data outputs are disabled.

Offset cancellation loop

A control loop connected between the limiting amplifier output and the differential amplifier input cancels the DC offset. The loop bandwidth is fixed internally at 30 kHz.

Loss-of-signal detection (LOS)

The LOS section detects an input signal level below a fixed threshold. The threshold is determined by the current through pin LOSTH. If this current is increased, the threshold level will rise. An external resistor between LOSTH and V_{CCA} can be used, or a current can be forced into LOSTH. The default value for the external resistor is 86 kΩ. In this case, the current through LOSTH will be approximately 17.4 μA since the voltage at pin LOSTH is regulated at 1.5 V below the supply voltage. This threshold corresponds to an input current of 0.96 μA. The ratio of LOSTH current to input current is thus approximately 18 : 1. When the input signal level falls below this threshold, the LOS (PECL compatible) and LOSTTL (TTL compatible) outputs go HIGH. The hysteresis is fixed internally at 3 dB. Response time is typically less than 20 μs.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+6	V
V_n	DC voltage			
	pin 7: IPhoto	–0.5	+1	V
	pin 14: RFTEST	–0.5	V_{CC} + 0.5	V
	pins 22, 23, 26 and 27: OUTPECL, OUTQPECL, LOS and LOSQ	V_{CC} – 2	V_{CC} + 0.5	V
	pins 18 and 19: OUTCML and OUTQCML	V_{CC} – 2	V_{CC} + 0.5	V
	pin 29: LOSTH	–0.5	V_{CC} + 0.5	V
	pin 10: BWC	–0.5	+3.2	V
	pin 31: AGC	–0.5	V_{CC} + 0.5	V
	pin 11: V_{ref}	–0.5	+3.2	V
	pin 4: DREF	–0.5	V_{CC} + 0.5	V
	pin 15: OUTSEL	–0.5	V_{CC} + 0.5	V
	pin 28: LOSTTL	–0.5	V_{CC} + 0.5	V
I_n	DC current			
	pin 7: IPhoto	–1	+2.5	mA
	pin 14: RFTEST	–2	+2	mA
	pins 22, 23, 26 and 27: OUTPECL, OUTQPECL, LOS and LOSQ	–25	+10	mA
	pins 18,19: OUTCML and OUTQCML	–15	+15	mA
	pin 29: LOSTH	–2	+2	mA
	pin 10: BWC	–1	+1	mA
	pin 31: AGC	–0.2	+0.2	mA
	pin 11: V_{ref}	–2	+2.5	mA
	pin 4: DREF	–2.5	+2.5	mA
	pin 15: OUTSEL	–0.5	+0.5	mA
	pin 28: LOSTTL	–16	+16	mA
P_{tot}	total power dissipation	–	600	mW
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	150	°C
T_{amb}	ambient temperature	–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point	tbf	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	tbf	K/W

CHARACTERISTICS

For typical values T_{amb} = 25 °C and V_{CC} = 5 V; minimum and maximum values are valid over the entire ambient temperature range and process spread.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		3	5	5.5	V
I_{CCD}	digital supply current	note 1	13	20	28	mA
		note 2	–	47	–	mA
		note 3	11	17	24	mA
I_{CCA}	analog supply current		24	36	51	mA
P_{tot}	total power dissipation		–	–	525	mW
T_j	junction temperature		–40	–	+110	°C
T_{amb}	ambient temperature		–40	+25	+85	°C
R_{tr}	small-signal transresistance of the receiver	measured differentially at PECL outputs	–	1800	–	kΩ
		measured differentially at CML outputs	–	1100	–	kΩ
$f_{-3dB(h)}$	high frequency –3dB point	pin BWC left unconnected; note 4	–	470	–	MHz
$f_{-3dB(l)}$	low frequency –3dB point		20	30	40	kHz
$I_{i(IPhoto)(p-p)}$	input current on pin IPhoto (peak-to-peak value)	V_{CC} = 5 V	–400	+4	+1500	µA
		V_{CC} = 3.3 V	–400	+4	+500	µA
$V_{bias(IPhoto)}$	input bias voltage on pin IPhoto		720	800	970	mV
$I_{n(tot)}$	total integrated RMS noise current over bandwidth (referenced to input)	C_i = 1.2 pF; note 5				
		Δf = 311 MHz	–	55	–	nA
		Δf = 450 MHz	–	80	–	nA
		Δf = 622 MHz	–	120	–	nA
PSRR	power supply rejection ratio at V_{CC}	measured differentially; note 6				
		f = 100 kHz to 10 MHz	–	1	2	µA/V
		f = 10 MHz to 100 MHz	–	2	5	µA/V
		f = 100 MHz to 1 GHz	–	5	100	µA/V
$\Delta R_{tr}/\Delta t$	AGC loop constant		–	1	–	dB/ms
PECL outputs: OUTPECL and OUTQPECL						
V_{OL}	LOW-level output voltage	50 Ω to V_{CC} – 2 V	V_{CC} – 1100	–	V_{CC} – 900	mV
V_{OH}	HIGH-level output voltage	50 Ω to V_{CC} – 2 V	V_{CC} – 1840	–	V_{CC} – 1620	mV
V_{OO}	differential output offset voltage		–10	–	+10	mV
t_r	rise time	20% to 80%	–	200	300	ps
t_f	fall time	80% to 20%	–	140	250	ps

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PECL outputs: LOS and LOSQ						
V_{OL}	LOW-level output voltage	50 Ω to V_{CC} – 2 V	V_{CC} – 1100	–	V_{CC} – 900	mV
V_{OH}	HIGH-level output voltage	50 Ω to V_{CC} – 2 V	V_{CC} – 1840	–	V_{CC} – 1620	mV
V_{OO}	differential output offset voltage		–10	–	+10	mV
t_r	rise time	20% to 80%	–	–	600	ns
t_f	fall time	80% to 20%	–	–	200	ns
CML outputs: OUTCML and OUTQCML						
V_O	single ended output voltage	50 Ω to V_{CC}	V_{CC} – 260	–	V_{CC}	mV
$V_{o(se)(p-p)}$	single-ended output voltage (peak-to-peak value)	50 Ω to V_{CC}	150	200	260	mV
V_{OO}	differential output offset voltage	50 Ω to V_{CC}	–10	–	+10	mV
R_o	single ended output resistance		80	100	120	Ω
t_r	rise time	20% to 80%; 50 Ω, 1 pF load	–	92	–	ps
t_f	fall time	80% to 20%; 50 Ω, 1 pF load	–	62	–	ps
CMOS input: OUTSEL						
V_{IL}	LOW-level input voltage		–	0.4	0.8	V
V_{IH}	HIGH-level input voltage		V_{CC} – 1	V_{CC} – 0.5	–	V
CMOS output: LOSTTL						
V_{OL}	LOW-level output voltage		0	–	0.2	V
V_{OH}	HIGH-level output voltage		V_{CC} – 0.2	–	V_{CC}	V

Notes

1. OUTPECL, OUTQPECL, OUTCML, OUTQCML, LOS and LOSQ outputs are left unconnected. OUTPECL and OUTQPECL outputs are active.
2. OUTPECL and OUTQPECL outputs are terminated with 50 Ω to V_T. V_T is an external termination voltage for PECL outputs and is 2 V below the supply voltage. OUTCML, OUTQCML, LOS and LOSQ outputs are left unconnected
3. OUTCML and OUTQCML outputs are terminated with 50 Ω to V_{CCD}; CML outputs are active. OUTPECL, OUTQPECL, LOS and LOSQ outputs are left unconnected
4. The bandwidth is set to 470 MHz by default. It can be varied between 300 and 600 MHz by adjusting the voltage at pin BWC.
5. All $I_{n(tot)}$ measurements were made with an input capacitance of C_i = 1.2 pF. This was comprised of 0.7 pF for the photodiode itself, with 0.3 pF allowed for the PCB layout and 0.2 pF intrinsic to the package.
6. PSRR is defined as the ratio of the equivalent current change at the input (ΔI_{IPhoto}) to a change in supply voltage:

   $$PSRR = \frac{\Delta I_{IPhoto}}{\Delta V_{CC}}$$

   For example, a 1 mV disturbance on V_{CC} at 10 MHz will typically generate the equivalent of 2 nA extra photodiode current.

APPLICATION INFORMATION

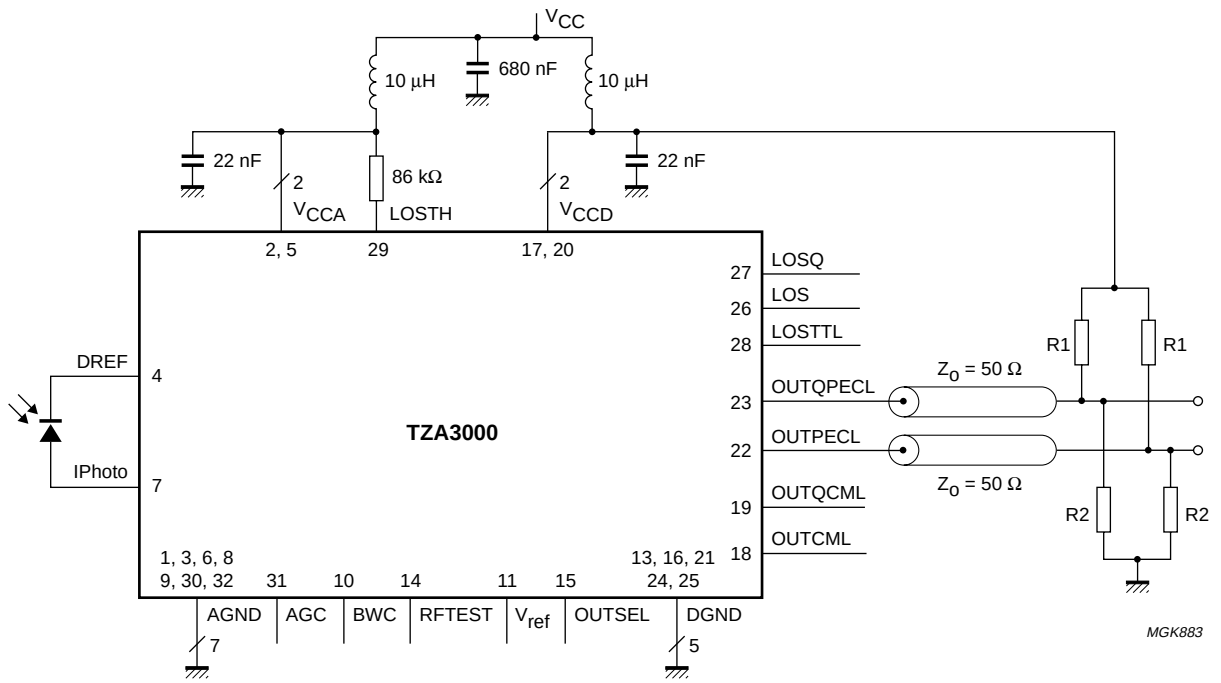


Fig.4 Application diagram: PECL data outputs active.

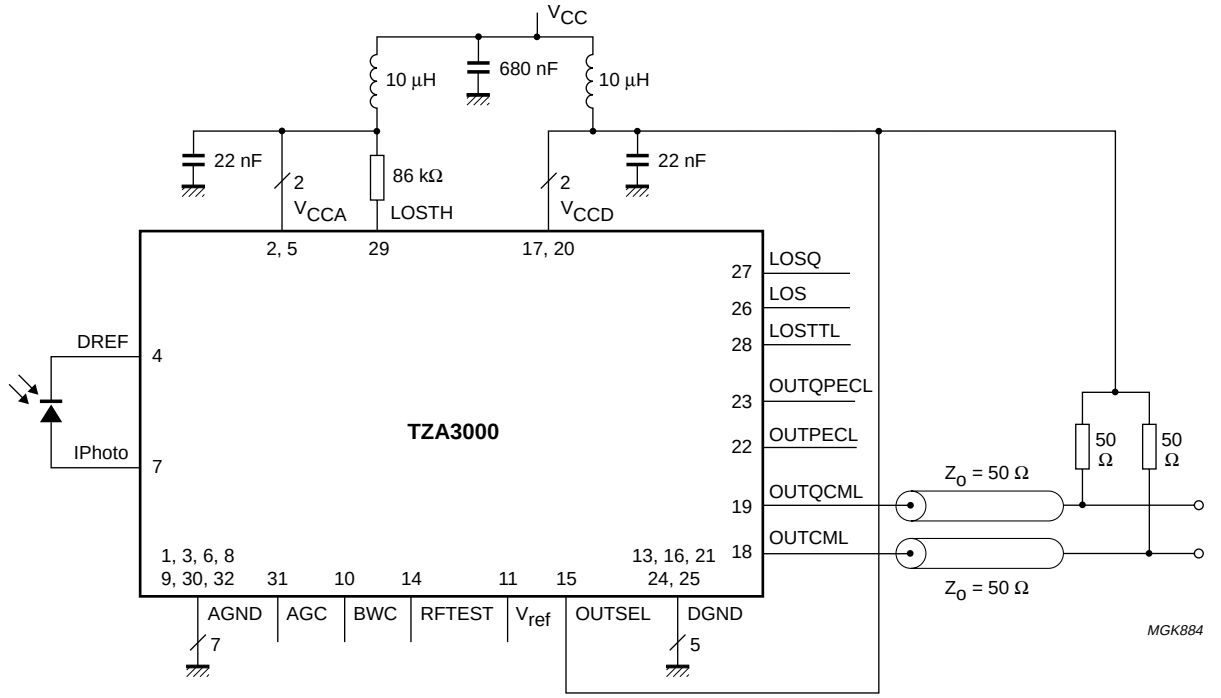


Fig.5 Application diagram: CML data outputs active.

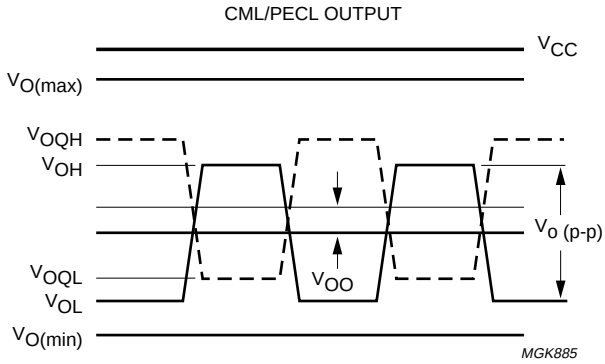
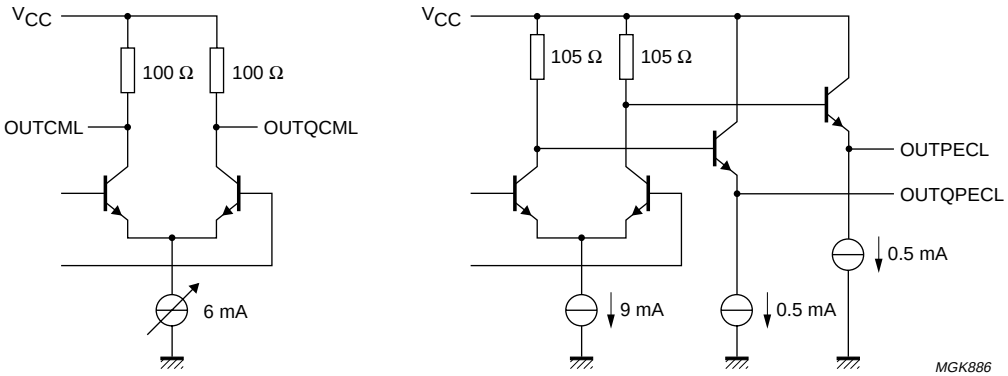


Fig.6 Logic level symbol definitions for CML and PECL.



a. CML. b. PECL.

Fig.7 Output circuits.

PECL outputs: OUTPECL (22), OUTQPECL (23), LOS (26) and LOSQ (27)

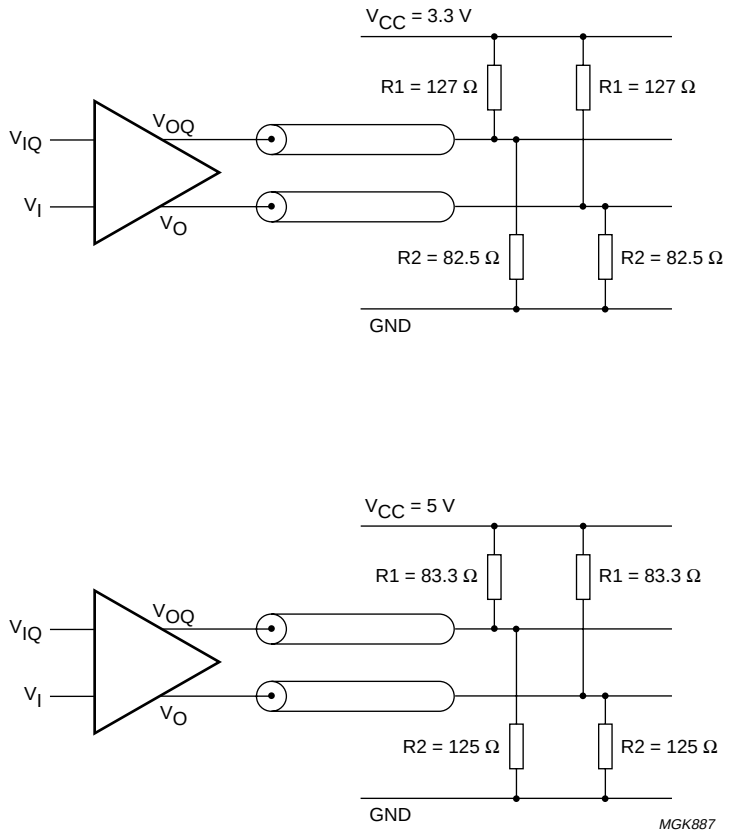


Fig.8 PECL termination schemes.

CML outputs: OUTCML (18) and OUTQCML (19)

The output impedance of the CML output driver is 100 Ω (see Figs 7 and 9), which doesn't match the characteristic impedance of the strip line. While this means that the reflections of some incident edges will arrive at the driver output on the PCB, this value was selected to reduce power dissipation inside the IC. The parallel combination of 100 Ω and 50 Ω (33 Ω) will generate a signal swing of 200 mV peak-to-peak (single sided) with a tail current of 6 mA. If the output impedance was 50 Ω rather than 100 Ω, an 8 mA tail current would be needed to generate the same voltage swing. This would increase power dissipation by 33%.

If necessary, the output impedance of the generator can be matched to the line impedance by connecting an external 100 Ω resistor in parallel with the output as shown in Fig.10. The magnitude of the output voltage swing will not change due to adaptive regulation. However, power dissipation will increase by 33%.

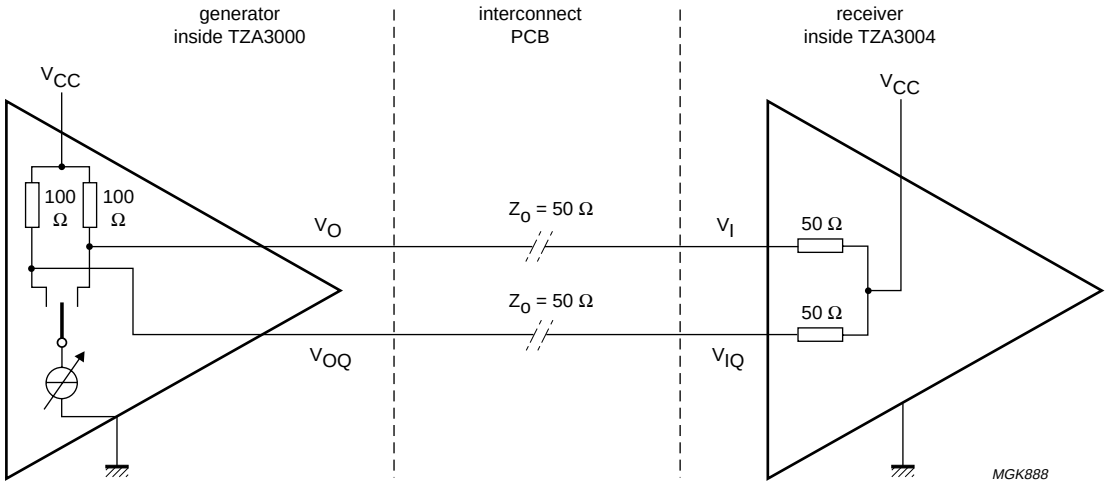


Fig.9 CML interface circuit without matched impedance; low power dissipation.

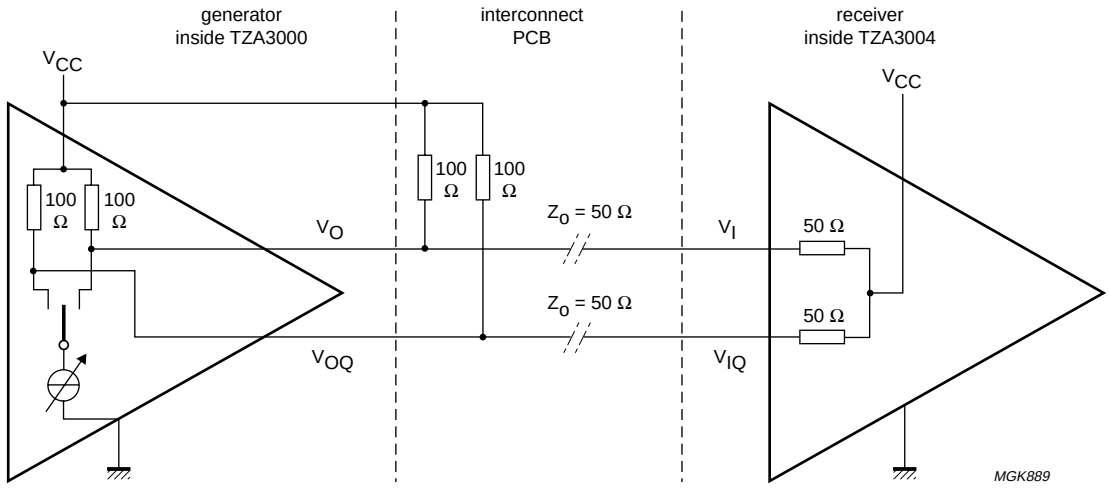
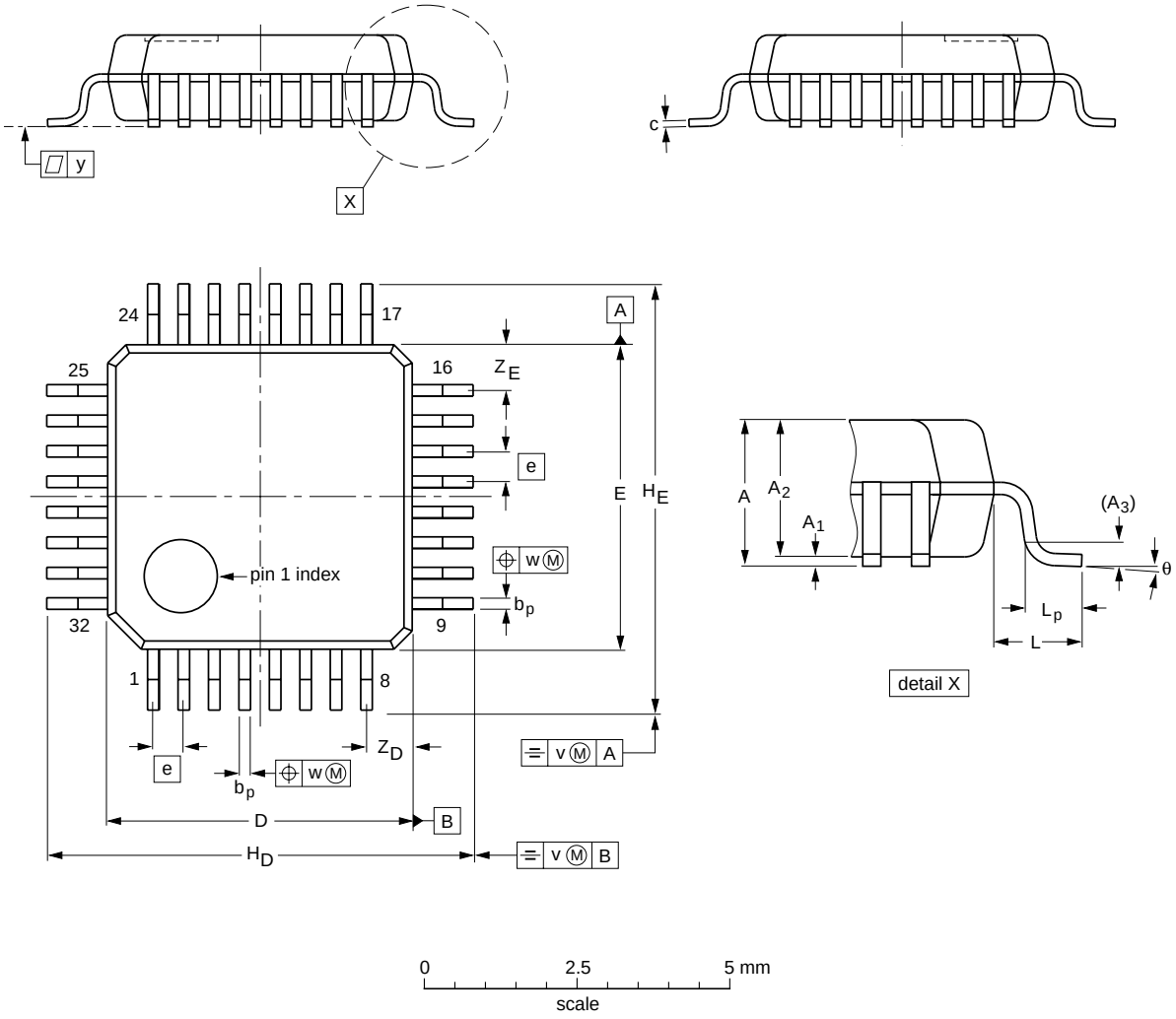


Fig.10 CML interface circuit with matched impedance; higher power dissipation.

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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